Curriculum Vitae et Studiorum

Giacomo Valente

1 Personal

Date and Place of birth	:	6th of August 1987, Pescara (PE)
Address	:	Viale Duca degli Abruzzi 2, 67100 - L'Aquila (AQ), Italy
Mobile Phone	:	+39 349 0685728
E-mail	:	giacomo.valente@univaq.it
	:	giakomo.87v@gmail.com

2 Current Position and Education

Current Position:

- *May 2021 – current*: Post-Doc Research Fellow at Department of Information Engineering, Computer Science and Mathematics (DISIM) at University of L'Aquila. Title of the project "Design methodologies for monitoring systems targeting heterogeneous platforms for edge-computing".

Previous Positions:

- *March 2020 – February 2021*: Post-Doc Research Fellow at Center of Excellence DEWS (Design Methodologies of Embedded controllers, Wireless interconnect and Systems-on-chip) at University of L'Aquila. Title of the project "HW-mechanism for run-time monitoring of embedded systems".

- *January 2018 - December 2019:* Post-Doc Research Fellow at Center of Excellence DEWS at University of L'Aquila. Title of the project "Methodologies, tool and HW/SW mechanisms for run-time monitoring of embedded systems".

- *November 2017 – December 2017.* Scientific collaboration with DEWS Center of Excellence at University of L'Aquila in the context of the project ECSEL-JU 737494 MegaMaRt2 for the design and implementation of a monitoring system able to provide run-time information with a specific trace format, described by a defined meta-model.

- *November 2014 - October 2017:* **PhD in "Information and Communication Technology"** at Department of Information Engineering, Computer Science and Mathematics (DISIM) at University of L'Aquila.

- *July 2015:* Scientific collaboration with DEWS Center of Excellence at University of L'Aquila in the context of the project Artemis-JU 295371 CRAFTERS for the development of a HW/SW co-design tool.

- *April 2014 - October 2014:* Scientific collaboration with DEWS Center of Excellence at University of L'Aquila in the context of the project Artemis-JU 295371 CRAFTERS for the development of a hardware monitoring system for heterogeneous SoC architectures.

3 Education and Qualifications

- *July 2020.* PhD School "2020 International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems" (ACACES), organized by HIPEAC Network; main topic: design for reliability and design of accelerators for embedded systems targeting FPGAs.

- *November 2014 - October 2017.* **Ph.D. in "Information and Communication Technology"** at University of L'Aquila. Title of the Thesis "A HW/SW Unified approach for Embedded Systems Monitoring", defended the 14th of May 2018.

- *September 2019, 2018, 2017 (3 editions).* PhD School "Cyber-Physical Systems Summer School", organized by University of Sassari, with lectures on the topic of safety, reliability, low-power design, contract-based design, and self-adaptive Cyber-Physical systems.

- *March 2018.* PhD School "2nd ARVI COST School on Run-time Verification", organized by INRIA; main topic: run-time verification and monitoring of Cyber-Physical systems.

- *July 2016.* PhD School "2016 Open Space Programming Language (SPL) Summer School", organized by Imperial College; main topic: hardware description languages to describe dataflow modelled systems.

- *22nd of July 2014.* **Laurea Magistrale (M.Sc. equivalent) with Laude** in Electronic Engineering at University of L'Aquila. Title of the Thesis "FPGA hardware profiler design and implementation for monitoring multiprocessor SoC memory accesses".

- *July 2011.* Laurea (B.Sc. equivalent) in Electronic Engineering at University of L'Aquila. Title of the Thesis "Ultra-Wideband systems Radio Frequency Identification".

- *June 2006.* Diploma in Industrial Engineering in Electronic and Telecommunications, at "Istituto Tecnico Industriale Statate (ITIS) Luigi di Savoia", Chieti.

- *Foreign Languages.* In the following table there are the levels compliant with the European standard for foreign languages (https://europass.cedefop.europa.eu/resources/european-language-levels-cefr).

	Understanding	Speaking	Writing
English	B2	B2	B2
French	B1	B1	B1

Table 1: Foreign languages.

4 Scientific Research activity

I am author and co-author of c.a. 50 national and international scientific peer-reviewed publications. The list of publications is reported in Section 6. My scientific production has obtained 130 citations with Hirsch index equal to 7 (Scopus) and 154 citations with Hirsch index equal to 8 (Google Scholar), last access 21st of October 2021.

4.1 Results of Scientific Research activity

My main research thrusts are on the design of embedded systems and electronic design automation. To this end, I mainly worked on three areas, all targeting on-chip platforms: (i) FPGA Dynamic Partial Reconfiguration (DPR) for hard real-time systems [2,8,11,22]; (ii) run-time system analysis (monitoring systems, MONICA tool [1]) [1, 3, 5–7, 9, 10, 13–15, 19–21, 26, 30–32, 36–38, 40–45, 48, 49]; (iii) HW/SW Co-design (Hepsycode tool [2]) [4, 12, 16–18, 23–25, 27–29, 33–35, 39, 46, 47].

All the activities have been and are currently developed in collaboration with research institutions and industries. In the following, results of my research activities are briefly reported.

4.1.1 DPR for real-time systems

The usage of custom circuits on reconfigurable architectures (e.g., FPGAs) allows a better control of the worst-case bound of tasks under execution, making them a candidate target for real-time systems. FPGAs also offer the capability, through the DPR process, of changing hardware at run-time, unlocking new design opportunities. To this end, I proposed a model to safely estimate the worst-case bound of the DPR process in a platform-independent way [2, 22], and a framework that allows to better exploit the features of modern SoC architectures by hard real-time designers [8,11].

4.1.2 On-chip monitoring systems

Embedded systems are characterized by the simultaneous optimization of many design metrics, that have led to the adoption of complex on-chip architectures. In this context, the development of on-chip monitoring systems is a key parameter to characterize the system at run-time. I first proposed, in a Ph.D. forum [7], a framework to support designers on the implementation of monitoring systems for embedded systems developed on FPGA. Then, the framework has been enriched with a high flexible hardware monitoring system [1, 19, 30]. The developed framework has been validated into real heterogeneous targets SoCs architectures, involving different use-cases from Industry [4,5,14,15] and Academic [26, 27].

4.1.3 HW/SW Co-design Tools

The area of HW/SW Co-design has been covered by my researches. In particular, I operated both on providing support for designers to select final target platforms and on implementing applications, keeping into account their functional and non-functional requirements. In particular, requirements span among different categories: speed-up requirements starting from a single-thread execution [4, 25], real-time and mixed-criticality requirements [16, 18, 23, 24, 28, 29, 34, 35, 39].

4.2 Scientific Collaborations

- *June 2021 – current.* Scientific collaboration with Trevize company, sited in Vasto (Chieti). The collaboration is on the topic of efficient implementation of a neural network for age and gender recognition on resource constrained devices (for edge-computing applications in Cyber-Physical Systems), done in the context of the European project ECSEL-JU 877056 FRACTAL.

- *July 2021 – current.* Scientific collaboration with MODIS company, sited in Rome. The collaboration is on the topic of techniques to efficient implement neural networks on resource

[1] https://monicatool.cloud/
[2] https://www.hepsycode.com/

constrained devices (for edge-computing applications in Cyber-Physical Systems), done in the context of the European project ECSEL-JU 877056 FRACTAL.

- *June 2021 – current.* Scientific collaboration with the "Real-Time Systems" (ReTiS) research laboratory at Scuola Superiore Sant'Anna of Pisa. The collaboration is on the topic of development of models to safely estimate the worst-case bound of the DPR process on FPGA, when multiple actors share the same resource. The collaboration led to organizing a Ph.D. visiting (Ph.D. student Gabriella D'Andrea at DISIM Department, University of L'Aquila) at ReTiS Lab.

- *January 2020 – current.* Scientific collaboration with"Grupo de Ingeniería Microelectrónica" research laboratory, at TEISA department of University of Cantabria (Spain). The collaboration is on the topic of efficient implementation of Cyber-Physical System, and led to publication of a scientific paper at international conference [13] and to the writing of a funded European project ((H2020-ECSEL-2020 101007350 AIDOaRT).

- *September 2017 – current.* Scientific collaboration with "IDEA Lab" research laboratory at University of Sassari and research laboratory "Microelectronics and Bioengineering Lab" at University of Cagliari. The collaboration is on the topic of development of a tool to automate the implementation of FPGA accelerators, and led to the publication of one journal paper [1], one conference paper [9], one invited talk for the PROSSIMO project [44], writing of one funder European project (ECSEL-JU 783162 Fitoptivis), and presentation of several posters at international conferences.

- *January 2019 – December 2019.* Scientific collaboration with electronic engineering research laboratory, Department of Industrial and Information Engineering and Economics (DIIIE) at University of L'Aquila. The collaboration was on the topic of development of a framework for the efficient implementation of Powerlink protocol compliant interfaces, and led to the publication of 1 journal paper [3].

- *September 2018 – September 2019.* Scientific collaboration with Sundance company, sited in United Kingdom. The collaboration was in the context of development of monitoring systems to monitor the power of embedded platforms.

- *March 2017 – June 2017.* Visiting Ph.D. at "Reconfiguration Computing Lab" at Simon Fraser University (Vancouver, BC, Canada) for the development of the following activities:

  - porting of necessary libraries to implement OpenMP based applications on an embedded multi-core processor (called PolyBlaze);
  - implementation of an indoor localization algorithm on PolyBlaze embedded multi-core processor on FPGA, using OpenMP.

- *September 2017 – April 2017.* Scientific collaboration with Rapita Systems company, sited in United Kingdom. The collaboration was performed in the context of development of unobtrusive on-chip monitoring systems to estimate the worst-case execution time, by means of measurement-based techniques. The collaboration led to one international conference paper [15], and happened in the context of the European project Artemis-JU 295371 CRAFTERS.

- *March 2015 - March 2017.* Scientific collaboration with Thales Italy company. The collaboration was performed in the context of development of an embedded platform for efficient implementation of indoor localization algorithms. The collaboration led to an international journal paper [4] and one international conference paper [19], and has been done in the context of the European project Artemis-JU 295371 CRAFTERS.

4.3 Scientific activities and scientific organization activities

4.3.1 Scientific activities

- *Invited Speaker for Summer School* – PhD School "CPSIoT 2021". Title of the talk "Dataflow-Based Toolchain for Adaptive Hardware Accelerators Deployment and Monitoring", Budva (Montenegro), 8 June 2021.
- *Invited Tutorial for Summer School*: PhD School "2020 Cyber-Physical Systems Summer School", organized by University of Sassari. Title of the tutorial - "Monitorable accelerators on FPGA", Pula, September 2020.
- *Invited Speaker for training day* – speaker for PROSSIMO project, Title of the talk - "Architetture eterogenee on-chip riconfigurabili: analisi, sviluppo e caratterizzazione del loro comportamento con sistemi di monitoring", Sassari, 18 February 2020.
- *Speaker*: DATE2021, DAC2021, HIPEAC2020, DATE2020, IWES2018, DAC2017, RTSI2016, PDP2016, IWES2016, DATE2016, WISES2015, FPL2015, DATE2015.
- *Scientific Reviewer*: Future Generation Computer Systems (Elsevier, international journal), Microprocessor and Microsystems (Elsevier, international journal), Computers in Biology and Medicine (Elsevier, international journal), International Symposium on Circuit and Systems (ISCAS, international conference), Research and Technologies for Society and Industry (RTSI, international conference), Mediterranean Embedded Computing Confence (MECO, international conference).

4.3.2 Scientific organization activities

- *Tutorial Organizer*: Title of the tutorial "HEPSYCODE: HW/SW Co-Design of Heterogeneous Parallel Dedicated Systems" at HIPEAC 2018 (January 2018, Manchester) and HIPEAC 2019 (January 2019, Valencia) international conference.

4.4 Scientific involvement in international and national research projects

- *Scientific Collaboration* – "ECSEL-JU 877056 FRACTAL Cognitive Fractal and Secure Edge Based On Unique Open-Safe-Reliable-Low Power Hardware Platform Node" project. I am currently working on the University of L'Aquila internal activities related to the development of an edge-computing platform able to execute artificial intelligence applications in a distributed way, without accessing the cloud.
- *Task Leader* – "ECSEL-JU 783162 Fitoptivis - From the cloud to the edge - smart Integration and Optimization Technologies for highly efficient Image and Video processing Systems" project. I am currently Task Leader of the Task 4.2: Model driven monitoring, profiling and measuring, where I am coordinating all the activities for the development of a framework for the monitoring of Cyber-Physical Systems implemented on cloud-edge platforms. I have been editor of D4.3 and D4.4 Deliverables, both titled "Monitoring, profiling, measuring and reconfiguration support for real time quality and resource management".
- *Scientific Collaboration* – "ECSEL-JU 737494 MegaMaRt2 – Mega-Modelling at Run-time" project. I worked on the University of L'Aquila scientific activities for the development of a monitoring system for run-time verification.

- *Scientific Collaboration* – "Artemis-JU 295371 CRAFTERS - ConstRaint and Application driven Framework for Tailoring Embedded Real-time Systems" project. I worked on the University of L'Aquila scientific actitivies for the development of monitoring systems for profiling and worst-case execution time estimation.

- *Advisory Board Member* – "Horizon 2020 688403 TULIPP Toward Ubiquitous Low-Power Image Processing Platforms" project.

4.5 Editor for journals

- *Guest Editor* – (1) Special Issue "Electronic System-Level HW/SW Co-Design of Power-Aware Embedded Systems" for the Journal of Low Power Electronics and Applications (MDPI) (international journal). (2) Special Issue "New Trends in Embedded System and Technology" for the Journal of Applied Sciences (MDPI) (international journal).

4.6 Honours and awards for scientific activities

- *Best Conference Poster*. Best poster award at international conference DSD 2018, August 2018, for the poster "Design Space Exploration for Mixed-Criticality Embedded Systems considering Hypervisor-based SW Partitions".

- *Best Conference Paper*. Best paper award at the international conference ECYPS 2018, June 2018, for the paper "HEPSIM: an ESL HW/SW Co-Simulator/Analysis Tool for Heterogeneous Parallel Embedded System".

- *Award for research project*. IEEE Young Professional award for the proposal"Adaptive Profiling Hardware Sub-system" at the International Conference RTSI 2016, September 2016.

4.7 Tutoring for PhD Students

- *2018 - current*: technical responsible for the PhD student in "Information and Communication Technology" Gabriella D'Andrea, at DISIM department, University of L'Aquila.

4.8 Membership

- *2015 - current*: member of Hipeac European network (High Performance and Embedded Architecture and Compilation), for which I contributed with different posters, presentations, and articles on newsletter about my research activities.

5 Teaching activities

5.1 Academic teaching activity

- *2021*. Seminar at "Basi di Dati 2" course, Master of Science curriculum in Computer Engineering, University of L'Aquila.

- *2019*. Co-lecturer for "Digital Electronic Systems" course (6 CFU/) CFU, 60 hours), Master of Science curriculum in Telecommunication Engineering, University of L'Aquila (1 edition).

- *2014-2021*. Assistant professor for "Embedded Systems" course (1 CFU/9CFU, 10 hours), Master of Science curriculum in Telecommunication Engineering, University of L'Aquila (8 editions).

- *2019*. Assistant professor for "Elettronica dei Sistemi Digitali 2" course (1 CFU/9 CFU, 10 hours), Master of Science curriculum in Electronic Engineering, University of L'Aquila (1 edition).
- *2017-2018*. Assistant professor for "Digital Electronic Systems" course (3 CFU/6 CFU, 30 hours), Master of Science curriculum in Telecommunication Engineering, University of L'Aquila (2 editions).
- *2017-2018*. Seminar at"Elettronica dei Sistemi Digitali 2" course, Master of Science curriculum in Electronic Engineering, University of L'Aquila (2 editions).

5.2 Tutoring and co-tutoring

Co-tutoring of 10 Bachelor and Master of Science Thesis at University of L'Aquila and responsible for technical aspect of the ICT Ph.D student Gabriella D'Andrea (XXXIV cycle) at University od L'Aquila.

5.3 Other teaching activities

- *2021* – Invited talk at PhD School "CPSIoT 2021". Title of the talk "Dataflow-Based Toolchain for Adaptive Hardware Accelerators Deployment and Monitoring", Budva (Montenegro).
- *2020*: Invited tutorial at PhD school "2020 Cyber-Physical Systems Summer School", organized by University of Sassari. Title of the tutorial - "Monitorable accelerators on FPGA".
- *2020* – speaker for PROSSIMO project, Title of the talk - "Architetture eterogenee on-chip riconfigurabili: analisi, sviluppo e caratterizzazione del loro comportamento con sistemi di monitoring".
- *2015* - Course " Parallel Programming Libraries" at Thales Italy company, 7 hours.

6 Publication List

References

[1] G. Valente, T. Fanni, C. Sau, T. D. Mascio, L. Pomante, and F. Palumbo, "A composable monitoring system for heterogeneous embedded platforms," *ACM Trans. Embed. Comput. Syst.*, vol. 20, no. 5, 2021. [Online]. Available: https://doi.org/10.1145/3461647

[2] G. Valente, T. Di Mascio, G. D'Andrea, and L. Pomante, "Dynamic partial reconfiguration profitability for real-time systems," *IEEE Embedded Systems Letters*, pp. 1–1, 2020.

[3] G. Valente, V. Muttillo, M. Muttillo, G. Barile, A. Leoni, W. Tiberti, and L. Pomante, "Spof—slave powerlink on fpga for smart sensors and actuators interfacing for industry 4.0 applications," *Energies*, vol. 12, no. 9, 2019. [Online]. Available: https://www.mdpi.com/1996-1073/12/9/1633

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[6] G. Valente, P. Giammatteo, V. Muttillo, L. Pomante, and T. D. Mascio, "A lightweight , hardware-based support for isolation in mixed-criticality Network-on-Chip architectures," *Advances in Science, Technology and Engineering Systems Journal*, vol. 4, no. 4, pp. 561–573, 2019.

[7] G. Valente, "A framework for integrated monitoring of real-time embedded soc," in *25th International Conference on Field Programmable Logic and Applications (FPL)*, 2015, pp. 1–2.

[8] G. D'Andrea and G. Valente, "Work-in-progress: Cyber-physical systems and dynamic partial reconfiguration scalability: opportunities and challenges," in *2020 IEEE Real-Time Systems Symposium (RTSS)*, 2020, pp. 399–402.

[9] G. Valente, T. Fanni, C. Sau, and F. Di Battista, "Layering the monitoring action for improved flexibility and overhead control: work-in-progress," in *2020 International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, 2020, pp. 18–20.

[10] G. Valente, T. Di Mascio, L. Pomante, and V. Stoico, "An esl methodology for hw/sw co-design of monitorable embedded systems: the "design for monitorability" project - work-in-progress," in *2020 International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, 2020, pp. 40–42.

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[12] V. Muttillo, G. Valente, and L. Pomante, "Design space exploration for mixed-criticality embedded systems considering hypervisor-based sw partitions," in *2018 21st Euromicro Conference on Digital System Design (DSD)*, 2018, pp. 740–744.

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Intelligent Systems for Technology Enhanced Learning, 11th International Conference, F. De la Prieta, R. Gennari, M. Temperini, T. Di Mascio, P. Vittorini, Z. Kubincova, E. Popescu, D. Rua Carneiro, L. Lancia, and A. Addone, Eds. Cham: Springer International Publishing, 2022, pp. 54–64.

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Giacomo Valente